Realization of In-Band Full-Duplex Operation Using Bilateral Single-Sideband Frequency Conversion

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Abstract—CMOS-integrated in-band full-duplex (IBFD) operation in wireless links and cryogenic quantum platforms was previously enabled by magnetic-free circulators using the phase non-reciprocity of spatial-temporal modulation. In this paper, we present an alternative and simple integrated circuit scheme, that not only realizes non-reciprocal signal flows required for IBFD operations, but also improves the isolation performance by completely eliminating any chip-level TX-to-RX coupling. The above functions are enabled by performing a direction/frequency-independent, single-sideband down-conversion to the counter-propagating TX and RX signals, which creates opposite deviations of on-chip TX and RX down-conversion to the counter-propagating TX and RX signals, RX frequencies with respect to the antenna frequency. Such a principle also broadens the isolation bandwidth and enables integrated receiver down-mixing function. As a proof-of-concept, a 3.4–4.6-GHz front-end (30% fractional bandwidth) is implemented using a 65-nm bulk CMOS technology. The measured Tx-Rx isolation of the circuit is 32–51 dB at 300 K, and 14–29 dB at 4.2 K. The measured TX-ANT and ANT-RX insertion loss are 3.0 and 3.2 dB at 300 K, and 1.9 and 2.0 dB at 4.2 K. At 300 K, the measured TX-ANT and ANT-RX IIP3 are 29.5 and 27.6 dBm, respectively. The IBFD core of the chip occupies an area of 0.27 mm² and consumes 48 mW of DC power.

Index Terms—in-band full-duplex, magnetic-free circulator, non-reciprocal, bilateral frequency converter, isolation, coupling, wideband, cryo-CMOS.

I. INTRODUCTION

THE ever-increasing demands of wireless communication capacity and sensing capability call for RF systems with more efficient utilization of the congested electromagnetic spectrum. Compared with half-duplex modes, such as time-division duplex and frequency-division duplex, in-band full-duplex (IBFD) mode potentially doubles the spectral capacity and simplifies transmission protocols [1], [2]. Non-reciprocal electronic devices, such as isolator, gyrator, and circulator, are critical for full-duplex operations and have been extensively utilized in wireless data links and monostatic radars. In addition, circulator capable of operating under cryogenic condition is critical in quantum computing platforms, in which a non-reciprocal path is needed to extract the weak qubit measurement signal while blocking any inverse disturbance (e.g. pump signal of parametric amplifier) [3].

Shown in Fig. 1a, a circulator is a three-port device which delivers signal to the next port in a certain rotation. It enables an IBFD system where the transmit (TX) and receive (RX) signals have identical frequencies on the chip and share a single antenna. Conventional ferrite circulators based on Faraday rotation are bulky and cannot be integrated on a chip. Recently, magnetic-free circulators become attractive due to their compact size and compatibility with CMOS integrated circuit technologies [4]–[9]. Using time-variant devices, typically realized with clock-modulated switches in a N-path filter [2], such a component applies nonreciprocal phases to various signals at the same frequency, and then through a set of delay lines, it creates constructive addition of the desired signal at a certain port and cancellation of other undesired signals. It is noteworthy that the TX-to-RX isolation is a key parameter in a full-duplex system. A few imperfections may degrade the isolation. For example, the impedance mismatch at the antenna port causes part of the TX signal to be reflected to the RX port; this problem is normally alleviated by an impedance tuner at the antenna port. In the context of silicon integrated circuits, one critical limitation of isolation relates to the inevitable TX-to-RX coupling through the silicon substrate (especially in bulk CMOS processes with low substrate resistivity), power lines, inter-inductor magnetic crosstalk, etc. Fig. 1b shows the simulation on a silicon substrate with 10-Ω-cm conductivity: the coupling between inductors can be -20 dB when they are placed close to each other, indicating that a compact design is challenging in this scenario. Meanwhile, the isolation of these circulators relies on the aforementioned signal cancellation among separated transmission-line paths with desired phase shifting, which is narrowband in nature and is susceptible to non-ideal clocking and amplitude/phase mismatches among those paths.

In this paper, we present a fully-integrated IBFD front-end that utilizes a bilateral frequency converter (BFC) to realize non-reciprocity while addressing the above problems of circulator. As shown in Fig. 2, the two-port BFC is also driven by a modulation signal \( \omega_M \). Its one port is connected to the shared antenna (ANT), while the other port carries both the TX and RX signals. The key difference from the previous circulators is, although the TX and...
RX frequencies are identical at the antenna interface (i.e. \( \omega_{\text{ANT}}=\omega_0 \)), they are shifted to \( \omega_0+\omega_M \) and \( \omega_0-\omega_M \), respectively, inside the chip. The \( 2\omega_M \) separation is realized through a signal-direction-independent downconversion of the BFC. The TX and RX signals can be then physically separated by a high-pass filter (HPF) and a low-pass filter (LPF). One clear advantage of this scheme is that, due to such a frequency split, the aforementioned chip-level TX-to-RX coupling is eliminated. Our later analysis will also show that the high TX-RX isolation is wideband in nature and is robust against device mismatch, non-ideal clocking, etc.

A 4-GHz front-end that uses a 65-nm bulk CMOS technology and operates at both 300 K and 4.2 K is demonstrated as a proof-of-concept. Effective isolation across \( \sim30\% \) fractional bandwidth is obtained. This paper is organized as follows. In Section II, key properties of a BFC are analyzed. Section III then presents details of the circuit implementations for the 4-GHz front-end. In Section IV, the measurement results are shown. Finally, a conclusion with a performance comparison is given in Section V.

II. BILATERAL FREQUENCY CONVERTER WITH IRREVERSIBLE SPECTRAL SHIFT

The simplified schematic of a two-port BFC is shown in Fig. 3. It consists of four parallel paths, and each path is a series connection of one switch and one phase shifter. The switches are driven by modulation signals with quadrature phases, and introduce frequency and phase shifts to signals flowing along the paths. Albeit the resemblance to a passive single-sideband mixer, one important property of the presented topology that was unexplored before is its irreversible frequency conversion process, namely, the BFC always performs frequency downconversion regardless of the signal flow direction.

To understand that, we examine the phasor diagram of signals at various stages (i.e. A ~ E) of the schematic in Fig. 3. Fig. 4a shows the signal flowing from TX to ANT. For simplicity, only the positive frequency components are described in the following. At Stage A and B, the TX signal at \( \omega_{\text{TX}} \) is modulated with quadrature phases \( \varphi_M, i=1,2,3,4 \) of \( 0^\circ, 90^\circ, 180^\circ, \) and \( 270^\circ \) in Path 1 ~ 4, respectively. Thus, at Stage C, the two generated sideband frequency components \( (\omega_{\text{TX}}+\omega_M) \) and \( \omega_{\text{TX}}+\omega_M \) in Path \( i, i=1,2,3,4 \) carry the following phases:

\[
\begin{align*}
\varphi_{C, i} &= \varphi_M, \quad \text{for the upper sideband} \\
\varphi_{C, i} &= -\varphi_M, \quad \text{for the lower sideband}.
\end{align*}
\]

Next, these signals flow through the phase shifters. The values of the applied phases are selected to compensate the phase differences of the lower sideband signals (i.e. \( \Delta \varphi_1=\varphi_M, i \)) among the four paths, so that after the signal summation, only such lower sideband component is preserved at the ANT port. As a result, the TX signal is shifted down by \( \omega_M \) when flowing to ANT.

For a signal flowing backward (i.e. ANT to RX), similar phasor-diagram analysis can be applied. As shown in Fig. 4b, again only the lower sideband signal \( (\omega_{\text{ANT}}-\omega_M=\omega_{\text{RX}}) \) presents at Node A on the left. A key observation to straightforwardly explain such an irreversible frequency conversion is that the condition listed in (1) is always valid, regardless of the signal frequency and its flow direction through the switches. Similarly, the addition of the phase \( \Delta \varphi \) by the phase shifters is also independent of the signal frequency and direction.

\[\text{For simplicity of the illustration, we assume that when a signal passes through a modulated switch, only the upper and lower sides remain, while the component at the original signal frequency vanishes. Strictly speaking, that is not true for the single-ended signaling in Fig. 3. But it does happen for the differential signaling in our actual design (Fig. 5).} \]
The above two-step manipulation then always leads to the in-phase summation of the lower-sideband component and out-of-phase cancellation of the upper-sideband component, hence irreversible downconversion. As a result, the TX and RX signals are higher and lower than \( \omega_{\text{ANT}} \) and \( \omega_{\text{M}} \), respectively, and can be easily diverted to two separate on-chip paths using a HPF for TX and a LPF for RX port. Although the presented scheme does not deliver the exactly same function as a conventional circulator, it still enables IBFD operation in light of the identical TX and RX frequencies at a shared antenna interface; meanwhile, the TX/RX frequency split eliminates any coupling between the TX and RX blocks on the same die.

As described in Section I, isolation in prior magnetic-free circulators relies on out-of-phase cancellation of TX signal within two different paths, and non-ideal clocking and device parameters lead to TX-to-RX leakage. Next, we discuss the robustness of our scheme against these factors. From the above analysis, we see that similar imperfect signal cancellation happens with the presence of (1) different signal loss within the four paths, due to the mismatches of switch transistors and phase shifters, and (2) non-ideal duty cycle and quadrature phases of the clock. Fortunately, as Fig. 4 indicates, although the above problems are inevitable, the un-cancelled TX-to-ANT residual at the ANT port are located at \( \omega_{\text{ANT}} + \omega_{\text{M}} \) and \( \omega_{\text{ANT}} + 2\omega_{\text{M}} \), which can be easily filtered. Similarly, for the ANT to RX direction, the residual is located at irrelevant locations of \( \omega_{\text{RX}} + \omega_{\text{M}} \) and \( \omega_{\text{RX}} + 2\omega_{\text{M}} \). Isolation performance is therefore not degraded at all. We also note that such robust isolation also applies to a broad operation band: although the desired phase \( \Delta \phi \) applied by a shifter only remains precise within a narrow band, the imperfect vector cancellation in Fig. 4 at large frequency offset does not lead to TX-to-RX leakage. This is in contrast to prior CMOS circulators, which are narrowband in nature.

The presented circuit has a few more advantages in addition to the improved isolation and bandwidth. Firstly, the presented circuit uses only one set of switches (as opposed to two in [4]–[9]) in the signal paths, thus the linearity is improved. Secondly, by choosing \( \omega_{\text{M}} \) to be close to \( \omega_{\text{0}} \), the circuit can also perform additional function of receiver down-mixing; as a result, a dedicated down-conversion mixer succeeding the RX port is no longer needed. Alternatively, the BFC can also be designed to perform frequency up-conversion, which then makes it possible to incorporate the function of up-mixer in standard transmitters.

III. A 4-GHz Prototype: Circuit Implementations

To demonstrate the presented IBFD scheme, a CMOS RF front-end with 4-GHz antenna frequency is prototyped. The full schematic of the chip is shown in Fig. 5. In this section, design details and simulation results are provided.

One goal of this design to showcase an integrated homodyne down-mixing function, and correspondingly, \( f_{\text{M}} \) is chosen to be \( f_{\text{M}} = 4 \text{ GHz} \), and hence \( f_{\text{TX}} \approx 8 \text{ GHz} \). To suppress undesired signal/clock feedthrough in the switches at \( f_{\text{TX}} \), \( f_{\text{ANT}} \) and \( f_{\text{M}} \), differential signaling is adopted in the circuit. Each differential switch pair in Fig. 5 has transistor size of \( 64 \mu m \times 0.06 \mu m \). A pair of MIM capacitors are used as the HPF at the TX port, and an L-C LPF is employed at the RX port. To facilitate the single-ended testing of the chip, two on-chip
Three-stage differential buffer, (b) locking-range of ILFD, (c) output phase noise with different duty cycle and (d) output phase errors of the modulation signal generator.

Fig. 8: Simulated (a) operation range of active balun with three-stage differential buffer, (b) locking-range of ILFD, (c) output phase noise with different duty cycle and (d) output phase errors of the modulation signal generator.

The modulator signal generator consists of one active balun, three-stage differential buffer, an injection-locked frequency divider (ILFD), and duty cycle tunable drivers as shown in Fig. 7. A self-biasing common-source/drain amplifier is used as the active balun. Due to its symmetric schematic and layout, the active balun performs a wide operation frequency. With the common-mode suppression provided by the subsequent three-stage differential buffer, the simulated output amplitude/phase errors of the active balun are shown in Fig. 8a. The divide-by-2 ILFD consists of two PMOS latches, an NMOS ring amplifier, and an NMOS injection network. The PMOS latches provide the negative resistance for the ring oscillator. This symmetric structure enables an ultra-wide operation range. The injection network has four end-to-end connected transistors formed a ring. The simulated locking-range can be as wide as 1~35 GHz when injection power is 4 dBm as shown in Fig. 8b. The duty cycle tunable driver works through tuning the input DC of the inverter. Since
the clock transition is steep, the duty cycle would not affect the output phase noise, as shown in Fig. 8c. With the symmetric layout, the simulated output phase errors are small across a wide operation frequency as shown in Fig. 8d. Therefore, this modulation signal generator can output 0.5/~12.5 GHz low phase noise clock signals with 20%/~80% tunable duty cycle.

In order to deal with the temperature variation in cryogenic measurement, this modulation signal generator is over-engineered. The full EM simulation is adopted for the BFC-based frond-end. As discussed in Section II, our circuit is robust against to the process-voltage-temperature (PVT) variations. The simulated TX-RX isolation of the frond-end with matched ANT port is shown in Fig. 9. The TX-RX isolation is better than 42 dB across the whole operation frequency. The isolation does not changed a lot when the threshold voltage $V_{th}$ of switches increases 0.1 V. The isolation is better than 34 dB when half switches increase 100% size. More importantly, even with 20° modulation signal mismatch, the isolation is still better than 30 dB.

IV. MEASUREMENT RESULTS

The BFC-based full-duplex chip is fabricated using TSMC 65-nm bulk CMOS technology. The die photo is shown in Fig. 10. The core front-end circuit including the quadrature coupler, switches, modulation signal generator, HPF and LPF occupies only 0.27 mm² area. When used in a complete wireless system, the baluns in our IFBD front-end are not needed, because the antenna and the TX/RX circuitry are normally differential. So to test the performance of the core circuit of the chip, standalone structures consisting of back-to-back ANT and TX baluns are also fabricated for de-embedding purpose. The off-chip balun at the RX port is also measured and de-embedded through a back-to-back structure on PCB. The chip is characterized at both room temperature (at ~300 K) and cryogenic temperature (at ~4.2 K). Fig. 11a shows the setup for ANT-to-RX measurement at room temperature. In this setup, the RF performance is tested through the probing on the high frequency pads (ANT, TX, and LO). The low-frequency RX differential ports are wire-bonded to the PCB and connected to an off-chip balun. Power supplies and bias voltages are also wire-bonded and supplied externally.

A Keysight PNA-X network analyzer (N5245B) with a mixer-measurement configuration is utilized. The LO port of the PNA delivers the ~8-GHz (2$f_M$) modulation. To test the TX-to-ANT transmission, the other two ports of the PNA (Port 1 and 2) for cross-frequency S-parameter measurement are connected to the TX and ANT ports, respectively, and the RX port is terminated with 50 Ω. The TX frequency is swept from 7.4 to 8.6 GHz. Shown in Fig. 12a are the measured S-parameters after de-embedding the loss of the baluns. The TX-to-ANT insertion loss extracted from $S_{21}$ ranges from 3.0 to 5.8 dB across the 30% fractional bandwidth. As expected, $S_{12}$ that represents the reverse insertion from ANT to TX is below -10 dB, hence non-reciprocity. Next, the two PNA ports (dubbed as Port 2 and Port 3) are connected to the ANT and RX ports, respectively, and the TX port is terminated with 50 Ω. The measured S-parameters are shown in Fig. 12b. The ANT-to-RX insertion loss extracted from $S_{32}$ ranges from 3.2~6.1 dB. Similarly to the above case, the reverse RX-to-ANT transmission ($S_{23}$) is below -10 dB. Lastly, the TX-to-RX isolation is tested by connecting the two PNA cross-frequency ports with the TX and RX ports,
respectively, while loading the probed ANT port with 50 Ω. Shown in Fig. 12c, across the 30% fractional bandwidth, the measured isolation ranges from 25.5 to 43 dB. Note that the balun loss which contributes to additional isolation has already been de-embedded. Similar to all other full-duplex systems, the wave reflection at the ANT port degrades the isolation performance. With impedance tuning at the ANT port, the measured isolation improves to 32 to 50 dB.

The setup shown in Fig. 11a is also used to test the noise figure (NF) performance of the chip. To emulate the full-duplex operation, an extra signal generator is also connected to the TX port to mimic a simultaneously transmitted TX power of 0 dBm. With the TX power off, the measured NF shown in Fig. 12d has a minimum value of 5.8 dB. With the TX power turned on, unlike the significant NF degradation in full-duplex mode in [5], we only observe <1 dB NF degradation at some baseband frequencies; that again illustrates excellent isolation between the TX and RX paths. It is important to note that, since the presented circuit performs the homodyne down-conversion, the noise at both the upperside and lowerside bands around \( f_{\text{ANT}} \) is folded to the RX baseband output. Therefore, the data shown in Fig. 12d are in fact the single-sideband noise figure (SSB NF), which assumes that the input signal only lies at one sideband around \( f_{\text{ANT}} \). That explains why the NF in Fig. 12d is on average ~3 dB larger than the insertion loss in Fig. 12b. The above noise folding problem can be addressed by filtering out the noise at one sideband around \( f_{\text{ANT}} \). The resultant minimum NF (also often called IEEE SSB NF) is then ~2.8 dB.

The linearity of the circuit is also measured by sweeping the input power of the setup. The measured results are given in Fig. 13, where the IIP3 for the TX-to-ANT and ANT-to-RX directions are 29.5 and 27.6 dBm, respectively.

To test the IBFD circuit performance under cryogenic condition, a setup shown in Fig. 11b is used, where the PCB with the wire-bonded chip is placed inside liquid helium (4.2 K) and is connected to the same Keysight PNA-X through cables. The measured results are shown in Fig. 14. Compared to the TX-to-ANT transmission at 300 K, the one at 4.2 K is improved to 1.9–4.2 dB (Fig. 14a), which is probably due to the higher mobility in the channel, higher substrate resistivity (hence lower leakage to substrate), and lower metal resistivity [11]. Similarly, the measured ANT-to-RX insertion loss is also improved to 2.0–5.3 dB at 4.2 K. Since the ANT port is connected through a bond wire in Fig. 11b, rather than probing, the bond wire inductance causes impedance mismatch that cannot be compensated by the impedance tuner. The associated wave reflection at ANT port therefore degrades the TX-to-RX isolation. Shown in Fig. 14c, the measured isolation
ranges from 14 to 29.5 dB across the whole operation band. The measured minimum SSB NF is 4.8 dB no matter whether the TX signal (0 dBm) is injected or not.

The power consumption of the chip, entirely from the modulation signal generator, is 48 mW at 300 K and 42.6 mW at 4.2 K.

V. CONCLUSION
A new concept using frequency conversions of two counter-propagating signals is demonstrated, which performs non-reciprocity similar to that in circulators and enables in-band full-duplex systems in CMOS. In this paper, a 4-GHz IBFD front-end is implemented to demonstrate this scheme. Its performance is summarized in TABLE I, along with a comparison with other state-of-the-art integrated circulators in CMOS. One notable advantage of our front-end is the high TX-RX isolation across a wide operation frequency thanks to the widely separated TX and RX frequencies and the robustness against path mismatch and non-ideal clocking. The noise figure is not affected by the normal TX signal in the full-duplex mode. Meanwhile, with only one set of switches in the signal path, high linearity is obtained without using a SOI or high-voltage CMOS process. As described in Section III, the integrated quadrature modulation signal generator is over-engineered, leading to higher DC power compared to some works in the table; the problem should be alleviated with a more optimized clock generator design or with a more advanced CMOS technology nodes. It is also worth mentioning that, due to the simple construction of the presented scheme, a highly compact circuit area, when normalized to the square of wavelength, is achieved.

ACKNOWLEDGMENT
The authors thank Kathleen Howard and Richard Hoft at Keysight for their generous support of testing equipment and instructions. Any opinions, findings, conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the United States Air Force.

REFERENCES


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TABLE I: Comparison with the State-of-the-Art Integrated Circulators in CMOS

<table>
<thead>
<tr>
<th></th>
<th>This Work</th>
<th>[12]</th>
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<td>300K</td>
<td>4.2K</td>
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<td>Frequency (GHz)</td>
<td>3.4–4.6</td>
<td>5.6–7.4</td>
<td>5.8–7.6</td>
<td>0.65–0.85</td>
<td>0.86–1.08</td>
<td>22.7–27.3</td>
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<td>Fractional Bandwidth</td>
<td>30%</td>
<td>28%</td>
<td>26.9%</td>
<td>26.7%</td>
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<td>18%</td>
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<td>Minimum Isolation (dB)</td>
<td>32</td>
<td>14</td>
<td>18</td>
<td>17</td>
<td>15</td>
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<td>Minimum TX-ANT Loss (dB)</td>
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<td>Minimum ANT-RX Loss (dB)</td>
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<td>2.9</td>
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<td>Noise Figure (dB)</td>
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<td>4.8/4.8 (a)</td>
<td>2.4</td>
<td>N.A.</td>
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<td>TX-ANT IIP3 (dbm)</td>
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<td>N.A.</td>
<td>&gt;18.7</td>
<td>&gt;18.1</td>
<td>27.5</td>
<td>50</td>
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<td>ANT-RX IIP3 (dbm)</td>
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<td>&gt;18.1</td>
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<td>RX Down-Mixing?</td>
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<td>DC Power (mW)</td>
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<td>42.6</td>
<td>12.4</td>
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<td>59</td>
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<td>25 (λ²/6390)</td>
<td>16.5 (λ²/5789)</td>
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<td>CMOS Technology</td>
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<td>65-nm Bulk</td>
<td>180-nm Bulk</td>
<td>45-nm SOI</td>
<td>45-nm SOI</td>
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</table>

(a) With TX off (0 dBm) and the homodyne RX down-conversion function included.

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