W-band Quadrupler based on Multi-Chip Module and Schottky Barrier Diodes

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Abstract. This paper reports a W-band solid-state quadrupler based on multi-chip module and nonlinear schottky barrier diodes. The quadruple consists of Q-band doubler and amplifier, branched-guide coupler and two parallel W-band doublers that are power-combined in-phase using T-juntion at output waveguide, and each W-band doubler channel includes two schottky barrier diodes featuring two anodes on a 127um-thick quartz substrate. The power-combined strategy decreases the size of W-band quadrupler to 56mm×33mm×20mm and increases the maximum stable output power by twice with regard to the traditional W-band doubler. The measured output power of the quadrupler is greater than 20mW over the 80 to 90 GHz and 40mW within 80.6 to 86.6 GHz with above 12% 3dB bandwidth when driven with 2mW input power at 300K. The spectrum of output signal is tested and analyzed to obtain the purity and noise performance of signal.

I. Introduction

Local oscillator sources are a crucial part of all high-frequency receivers and transmitter. Solid-state harmonic multipliers is a main way to obtain higher frequency\cite{1}. Compared with others approaches, Solid-state harmonic multipliers offer the possibility to produce high stable, high power capacity, low phase noise and broadband millimeter wave signals\cite{2}. Nearly, there are many reports about frequency doubler or tripler based on schottky barrier diodes\cite{3,4,5}. However, single frequency doubler or tripler always generates limited conversion efficiency and output power, as dedicated in equation (1), not enough to pump cascading terahertz frequency doubler.

\[ \frac{P_{nf}}{P_f} \leq \frac{1}{n^2}, \text{ } n \text{ is harmonic order} \] (1)

To solve this problem, researchers have attempted lots of technologies\cite{6,7,8,9,10}, while power–combined frequency multiplier based on T-junction or hybrid coupler is the reliable approaches. For efficient power combining, the increasing attention must be paid to keep two parallel paths well-matched despite fabrication and assembly tolerances and to minimize losses in dividing and recombining the signal. In this context, we present the design, fabrication and test results of a W-band quadrupler that includes Q-band doubler chip and amplifier chip, branched-guide coupler and two parallel W-band doublers with a total of four Shottky barrier diodes. The W-band quadrupler produces 40mW within 80.6 to 86.6 GHz when pumped with 2mW input power.

II. Scheme

The W-band quadrupler is based on multi-chip such as Q-band doubler and Q-band amplifier, and W-band schcottky diode doubler in a split-waveguide block design shown Fig. 1. The 20-22.5GHz input signal is doubled and amplified by Q-band doubler and amplifier chip aiming to increase the input power of W-band doubler. Meanwhile, due to series resistance, power saturation and thermal effect of Schottky diode, the conversion efficiency $\eta$ of frequency doubler is limited\cite{11}.

\[ \eta = \exp \left( -a \cdot \frac{f_{out}}{f_c} \right) \] (2)
where \( f_{\text{out}} \) is the output frequency, \( f_c \) is the dynamic cutoff frequency and \( a \) is a parameter related to the harmonic order of output and to the input drive level.

The amplified input signal is split into two paths by branched-guide coupler to evenly feed two identical W-band doublers each featuring two Schottky planar barrier diodes. The two W-band doublers are mounted in two independent and parallel channels that run between their respective input and output waveguides as shown in Fig. 1(b). The two output waveguides of two W-band doublers are combined by a compact T-junction. The T-junction is completed with a succession of waveguide step to provide broadband impedance matching.

![Diagram](image)

**Figure 1.** (a) Schematic drawing, (b) the bottom half of the W-band quadrupler

In the input channel, Q-band doubler and amplifier chip both need the +5V bias voltage provided bias circuit. The output power at 1dB compression point of Q-band amplifier is 23dBm through 475mA bias current. An E-plane probe located in the input channel couples nearly 400mW signal in the Q-band frequency to branched-guide coupler. The 3dB coupler has seven sections and the simulated flatness and insertion loss is less than 0.2dB and 0.15dB within 40-45GHz. The 400mW signal evenly pumps two identical W-band doublers by another two Q-band E-plane probes. The second harmonic produced by the diodes is coupled to the output waveguide by a W-band E-plane probe. The detail introduction of W-band doubler will be present in next section.

### III. Design And Simulation OF W-band Doubler

The W-band schottky diode doubler is based on quartz microstrip circuit designed originally for the 0.14THz frequency doubler[5]. The design methodology combines Agilent ADS non-linear harmonic balance simulation to optimize the performance of the circuit, with Ansoft HFSS 3-D EM simulation to accurately model the diode geometry and waveguide structure, as in [5]. The high-low impedance low-pass filter between E-plane probe and the diodes prevents the second harmonic from leaking into
input waveguide. To improve the doubler bandwidth, the real impedance matching in input and output port of varactor is implemented. Simultaneously, the DC bias needs to be applied to the diode by a low-pass filter and gold wire. According to [5], the DC bias voltage is fixed to 0V and DC port is connected to the ground directly without worsening the performance of the doubler and simplifying structure instead. The diodes are located on 127μm-thick quartz substrate, as shown in Fig. 2(a). 13.5% peak simulated efficiency of W-band doubler is achieved with this topology as depicted in Figure 2(b).

To avoid the risk of overdriving an anode and investigate the balancing of the anodes in input frequency, the input coupling efficiency of each anode is simulated, as shown in Fig. 3. The input coupling efficiency is defined as following[8],

$$\text{Coupling efficiency} = \frac{P_{\text{anode}(i)}}{P_{\text{in}}/N} \times 100\%$$ \hspace{1cm} (1)

where N is the numbers of the anodes. $P_{\text{anode}(i)}$ is the driving power of each anode at pumped frequency $f_p$, which can be defined by Fourier series of the anode voltage $V_i$ and the diode current $i_i$.

$$P_{\text{anode}(i)} = \frac{1}{2} V_i(f_p) \cdot i_i(f_p)$$ \hspace{1cm} (2)

Fig. 3 clearly indicates the coupling efficiency of each anode almost approximates to ideal taking into account the loss of circuit. That is the input signal is poured into schottky diode furthest in order to produce more second harmonic signal. Fig. 4 shows that the power combining of W-band doubler is consummate so that the power-combined doubber perform with almost identical conversion efficiency as the single W-band doubber expect with twice the output power.

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**Figure 2.** (a) Close-up photograph of single W-band doubler. (b) Simulated efficiency with 200mW of input power.

**Figure 3.** Input power coupling efficiency of each signal anode.
IV. Quadrupler Measurements

We assembled and tested two quadrupler blocks. The source used to test the quadrupler consisted of a synthesizer tuned in the 20-22.5GHz band with 3dBm (the input power has been correct for the loss of coaxial RF cable). For all the measurements, the input power of the quadruplers was limited on 3dBm and DC voltage bias circuit was kept on 6V.

A. Frequency sweep

The output power of the quadrupler was measured using the power meter. Their output powers range from 20mW to 50mW across 80-90GHz band, shown in Fig. 5. A 57mW peak output power at 83.5GHz and a 12% 3dB bandwidth have been measured when pumped with a 2mW constant input power across the measured frequency band. Form the measured data, the center frequency of the quadrupler slipped slight. The discrepancy of two blocks in output power attributed to the bias current variation of the Q-amplifier, of which one is 540mA and another 570mA. In table 1, there was some research result about the power-combined strategy of frequency multiplier. [6] and [7] in overseas research indicated the power-combined method could be feasible in higher frequency and compared with [8], [9] and [10], this work had distinct advantage on conversion efficiency and output power which built more powerful source in microwave oscillator to drive terahertz component.
### Table 1 State of the art power-combined schottky multipliers or tripler

<table>
<thead>
<tr>
<th>Design</th>
<th>Year</th>
<th>Frequency</th>
<th>Pout(mW)</th>
<th>Conversion Efficiency(%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[6]</td>
<td>2011</td>
<td>177-202GHz</td>
<td>10mW</td>
<td>6-10%</td>
</tr>
<tr>
<td>[8]</td>
<td>2013</td>
<td>75-110GHz</td>
<td>6-10mW</td>
<td>1.2-3.8%</td>
</tr>
<tr>
<td>[9]</td>
<td>2012</td>
<td>50-75GHz</td>
<td>2.5-7mW(simulation)</td>
<td>2.5-7%</td>
</tr>
<tr>
<td>[10]</td>
<td>2012</td>
<td>86-96GHz</td>
<td>4-8</td>
<td>3-8%</td>
</tr>
<tr>
<td>This paper</td>
<td>2014</td>
<td>76-90GHz</td>
<td>20-50mW</td>
<td>8-13%</td>
</tr>
</tbody>
</table>

**B. Spectral Analysis**

The spectrum of the output signal was analyzed with Agilent spectrum analyzer and an external W-band mixer used as down converter. Since the input power of the mixer was limited to 3dBm, the input power of the W-band quadrupler was adjust to -6dBm corresponding when we analyzed the spectral characteristic of the quadrupler. Figs 4(a) and (b) show the spectral line of the output signal in 85GHz and 80GHz. Theoretically, the phase noise of natural circuit would be degraded $20 \times \log(N)$, where $N$ is the order of multiplication. According to the measurements, the quadrupler had low phase noise across the measurement band. While in Figs 4(a), at an offset of 3 KHz, there was a parasitic and indelible clutter signal. The existing clutter signal may degrade the THz signal purity pumped by the quadrupler. When THz mixer is used to the front of the receiver, the purity of LO signal is fatal for the sensitivity. There are the following reasons of the clutter signal: (a) the purity of DC current is not enough to be block to RF signal and leak into RF channel. (b) the Q doubler chip introduces the clutter signal when doubles the input signal.

![Figure 4. Spectrum of the output signal (a) 85GHz. (b) 80GHz.](image-url)
V. Summary

The W-band quadrupler based on multi-chip module and schotty diodes has been successfully accomplished with nearly 50mW output power and 12% 3dB bandwidth. Two W-band power combined doubler produces approximately twice as much power without sacrificing efficiency or bandwidth compared with single W-band doubler. This approach represents an important steps towards increasing the LO power at W-band and reducing the size of solid-state LO chains. It could be potentially applied to higher frequency.

References


